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EXAMINER	
TRINH, MICHAEL MANH	
ART UNIT	**PAPER NUMBER**
2822	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/25/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/717,977	MOK ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 14-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-10 and 14-17* is/are rejected.

7)☒ Claim(s) *2* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/8/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's Amendment filed October 27, 2006. Claims 1-10,14-17 are pending.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

1. Claims 16-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Egitto et al (6,826,830).

Re claim 16, Egitto teaches (at Figs 13-25, col 29, line 47 through col 32; Fig 1-2; cols 4-18) a method for manufacturing a parallel multi-layer printed circuit board, comprising the steps of: forming a plurality of circuit layers, wherein the circuit layers comprise via holes (Figs 19,24); forming a plurality of insulating layers, wherein the insulating layers comprises via holes filled with a conductive paste 555 (Figs 23-25; Fig 2); alternately arranging the circuit layers 560,570 and insulating layers 580 (Fig 24); and pressing the circuit layers and insulating layers and filling the via holes of the circuit layers with the conductive paste 555 from the via holes of the insulating layers to electrically connect the insulating layers with the circuit layers (Figs 24-25). Re claim 17, wherein the via holes 563 of the circuit layers are not filled with the plating or with conductive paste before pressing (Figs 24-25; col 32, line 23 through col 33).

Claim Rejections - 35 USC § 103

2. Claims 1,9,14,15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Egitto et al (6,826,830) taken with Furui et al (5,258,094).

Re claims 1, Egitto teaches (at Figs 13-25, col 29, line 47 through col 32; Fig 1-2; cols 4-18) a method for manufacturing a parallel multi-layer printed circuit board, comprising the steps of: (A) forming a predetermined number of circuit layers, including the sub-steps of: (a) forming via holes through a copper stack plate (Figs 19,24); (b) plating surfaces of the copper stack plate and inner walls of the via holes with copper (Fig 19, col 30 line 60 through col 31); and (c) forming circuit patterns on the copper stack plate (Fig 19); (B) forming a predetermined number of insulating layers, including the sub-steps of: (a) forming via holes through a flat-type insulating material provided with release films 544,542 (Fig 21) attached to surfaces of the flat-

type insulating material; (b) filling the via holes with a conductive paste 555 (Figs 23-25,2); and (c) removing the release films 544,542 from the flat-type insulating material (Fig 23); (C) alternately arranging the circuit layers 560,570 and the insulating layers 580 at predetermined positions (Figs 24,2); (D) pressing the arranged circuit and insulating layers to fill via holes of circuit layers with a conductive paste 555 of the insulating layers (Figs 23-25), wherein circuit patterns 567,578 are formed on the outermost layers of a board obtained by pressing the circuit layers and the insulating layer (Fig 24-25). Re claims 14, Egitto teaches (at Figs 13-25, col 29, line 47 through col 32; Fig 1-2; cols 4-18) a method for manufacturing a parallel multi-layer printed circuit board, comprising the steps of: (A) forming a predetermined number of circuit layers, including the sub-steps of: (a) forming via holes through a copper stack plate (Figs 19,24); (b) plating surfaces of the copper stack plate and inner walls of the via holes with copper (Fig 19, col 30 line 60 through col 31); and (c) forming circuit patterns on the copper stack plate (Fig 19); (B) forming a predetermined number of insulating layers, including the sub-steps of: (a) forming via holes through a flat-type insulating material provided with release films 544,542 (Fig 21) attached to surfaces of the flat-type insulating material; (b) filling the via holes with a conductive paste 555 (Figs 23-25,2); and (c) removing the release films 544,542 from the flat-type insulating material (Fig 23); (C) alternately arranging the circuit layers 560,570 and the insulating layers 580 at predetermined positions (Figs 24,2); (D) pressing the arranged circuit and insulating layers and filling the via holes in the circuit layers with conductive paste 555 from the insulating layers (Figs 24-25), wherein circuit patterns 567,578 are formed on the outermost layers of a board obtained by pressing the circuit layers and the insulating layer (Fig 24-25) . Re claims 15, Egitto teaches (at Figs 13-25, col 29, line 47 through col 32; Fig 1-2; cols 4-18) a method for manufacturing a parallel multi-layer printed circuit board, comprising the steps of: (A) forming a predetermined number of circuit layers, including the sub-steps of: (a) forming via holes through a copper stack plate (Figs 19,24); (b) plating surfaces of the copper stack plate and inner walls of the via holes with copper without completely filling the via holes (Fig 19, col 30 line 60 through col 31); and (c) forming circuit patterns on the copper stack plate (Fig 19); (B) forming a predetermined number of insulating layers, including the sub-steps of: (a) forming via holes through a flat-type insulating material provided with release films 544,542 (Fig 21) attached to surfaces of the flat-type insulating material; (b) filling the via holes with a conductive

paste 555 (Figs 23-25,2); and (c) removing the release films 544,542 from the flat-type insulating material (Fig 23); (C) alternately arranging the circuit layers 560,570 and the insulating layers 580 at predetermined positions (Figs 24,2); (D) pressing the arranged circuit and insulating layers (Figs 24-25); and wherein circuit patterns 567,578 are formed on the outermost layers of a board obtained by pressing the circuit layers and the insulating layer (Fig 24-25). Re claim 9, wherein the conductive paste functions as a point contact-type conductive paste 555 (Fig 23).

Egitto teaches forming circuit patterns 567,578 on the circuit layers, before pressing (Figs 24-25); whereas, base claims 1,14,15 recite a step of forming circuit patterns on the outermost layers of a board obtained by pressing.

However, Furui teaches (at Figs 14-18; col 5, line 38 through col 6) forming circuit patterns 68,61,21,26,66,67 (Fig 17) on the outermost layers of a board 1 obtained by pressing the circuit layers 14,15 and the insulating layers 52 (Figs 14-17).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form multi-layer printed circuit board of Egitto by forming circuit patterns on the outermost layers of a board obtained by pressing the circuit layers and the insulating layers, as taught by Furui. This is because of the desirability to form desired circuit patterns on the outermost layer of the board obtained by pressing the circuit layer and the insulating layer, wherein desired circuit patterns on the board can be subsequently formed and made for a particular circuit connection.

3. Claims 1,3-5,7-10,14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (2004/0194303) taken with Egitto et al (6,826,830) and Furui et al (5,258,094).

Re base claims 1,14,15,16, Kim teaches (at Figs 3A-8; paragraphs 65 through 96) a method for manufacturing a parallel multi-layer printed circuit board, comprising the steps of: (A) forming a predetermined number of circuit layers, including the sub-steps of: (a) forming via holes 304 through a copper stack plate 302/303 (Figs 3A-3B); (b) plating surfaces of the copper stack plate and inner walls of the via holes with copper 305 (Fig 1C); and (c) forming circuit patterns 306 on the copper stack plate (Fig 1d; paragraph 72; 306a-306c in Fig 7); (B) forming a predetermined number of insulating layers, including the sub-steps of: (a) forming via holes 504 through a flat-type insulating material provided with release films 502 attached to surfaces of the

flat-type insulating material 503 (Figs 5A-5B); (b) filling the via holes with a conductive paste 505 (Fig 5C); and (c) removing the release films 502 the flat-type insulating material (Fig 5D; paragraphs 81-85); (C) alternately arranging the circuit layers and the insulating layers at predetermined positions (Fig 7, paragraphs 93-97); (D), wherein omitting the plugging process of the via holes 204 using the paste 206 is alternatively taught at (at paragraph 61; Figs 2D-2E), wherein by omitting or not fill the via holes 204 with plating or conductive paste 206 before pressing at Figs 7-8 (paragraphs 61-63,55-60); and pressing the arranged circuit and insulating layers and filling the via holes in the circuit layers with conductive paste (Fig 8) from the insulating layers, wherein circuit patterns 306a-306c from the plated copper 305 are formed on the outermost layers of a board obtained by pressing the circuit layers and the insulating layers (Figs 7,8, 3d). Re claim 3, wherein surface-treatment of the copper stack plate 105 is performed so as to increase an adhering force (paragraphs 16, 21,24; Figs 1A-1E). Re claims 4-5, further comprising the step of: (F) forming a target hole at the position of a target guide mark, serving as a reference point of drilling, on the circuit layers and the insulating layers (re claim 4); and, re claim 5) wherein the sub-step (a) of each of the steps (A) and (B) includes the step of: (a') forming a guide hole at the same position, serving as a reference point of interlayer matching, on the circuit layers and the insulating layers (paragraphs 95-96; page 7, right column, lines 7-18). Re claim 7, wherein the release film 502 a thickness of 20 to 30 microns (paragraph 82; Figs 5A-5B). Re claims 8-9, wherein the conductive paste is a metallic bond-type conductive paste 106/505 impregnated with a tin (Sn) component, or re claim 9, wherein the conductive paste is considered as a point contact-type conductive paste 106/505 (paragraphs 16,84). Re claim 10, wherein the flat-type insulating material includes a resin material in a c-stage, and resin layers in a b-stage respectively stacked on both surfaces of the resin material (paragraph 87; Figs 6A-6D,5A-5D). Re further claims 15, as similarly applied to claim 1 above, Kim also alternatively teaches (at paragraphs 60-61; Figs 2C-2E) about plating inner walls of the via holes with copper 205 without completely filling the via holes. Thereafter, as shown in Figure 7-8, arranging and pressing such circuit layers and the insulating layers are arranged and pressed to form a parallel multi-layer printed circuit board, wherein circuit patterns 306a-306c from the plated copper 305 are formed on the outermost layers of a board obtained by pressing the circuit layers and the insulating layers (Figs 7,8, 3d).

Re claims 1,14,16, Kim already teaches pressing the arranged circuit and insulating layers, but lacks to fill the via holes in the circuit layers with the conductive paste; and Re claims 1,14-16, after obtaining a board by pressing, forming circuit patterns on the outermost layers of a board.

However, Egitto teaches (at Figs 13-25, col 29, line 47 through col 32; Fig 1-2; cols 4-18) connecting the insulating layers to the circuit layers, wherein the conductive paste 555 filling the via holes of the insulating layers flows into the via holes of the circuit layers by pressing the arranged circuit and insulating layers (Figs 24-25), wherein circuit patterns 567,578 are formed on the outermost layers of a board obtained by pressing the circuit layers and the insulating layer (Fig 24-25). Furui teaches (at Figs 14-18; col 5, line 38 through col 6) forming circuit patterns 68,61,21,26,66,67 (Fig 17) on the outermost layers of a board 1 obtained by pressing the circuit layers 14,15 and the insulating layers 52 (Figs 14-17).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form multi-layer printed circuit board of Kim by pressing to flow conductive paste from the insulating layer to fill the via holes in the circuit layers during pressing, as taught by Egitto. This is because of the desirability to provide an electrical connection, wherein the conductive paste are flown into the via holes so that the layers can be effectively joined together. Also, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form multi-layer printed circuit board of Kim by forming circuit patterns on the outermost layers of a board obtained by pressing the circuit layers and the insulating layers, as taught by Furui. This is because of the desirability to form desired circuit patterns on the outermost layer of the board obtained by pressing the circuit layer and the insulating layer, wherein desired circuit patterns on the board can be subsequently formed and made for a particular circuit connection.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (2004/0194303) taken with Egitto et al (6,826,830) and Furui et al (5,258,094), as applied to claim 1 above and further of Hirose (6,613,986).

Kim and Egitto teach (at Figs 3A-8; paragraphs 65 through 96) a method for manufacturing a parallel multi-layer printed circuit as applied to claims 1,3-5,7-10 above.

Kim and Egitto lack mentioning buffing a portion of the conductive paste, flowing out from the via holes of the outmost layer, so as to remove the protruding portion of the conductive paste, after the step (C).

However, Hirose teaches (at Figs 24C-25B, col 29, lines 10-22; Figs 1A-2D; col 16, lines 46-55) to buffing a portion of the conductive paste, flowing out from the via holes of the outmost layer, so as to remove the protruding portion of the conductive paste.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to manufacture the printed circuit board of Kim and Egitto by buffing a portion of the conductive paste flowing out from the via holes of the outmost layer, as taught by Hirose. This is because of the desirability to remove the unwanted protruding portion of the conductive past flowing out form the via holes.

Allowable Subject Matter

5. As already of record, Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Amendment

** Applicant remarked (at 10/27/06 remark page 8, first paragraph) that "...the circuit patterns of step (E) cannot be confused with the circuit patterns of step (A)(c)...; therefore, it is clearly understood that the circuit patterns of step (E) does not refer to the circuit patterns in step (A)(c)...Furthermore, in step (E), the phrase 'circuit patterns' is not preceded by a definite article, such as "the"; therefore, it is clearly understood that the circuit patterns of step(E) do not refer to the circuit patterns in step (A)(c)". Accordingly, the rejection under 35 USC 112 rejection, second paragraph, is withdrawn as the circuit patterns of step (E) and the circuit patterns of step (A)(c) are two different circuit patterns, wherein the circuit patterns of step (E) does not refer to the circuit patterns in step (A)(c). In general, a modifier such as first, second, etc., can be additionally used for identifying different circuit patterns (e.g. first circuit patterns, second circuit patterns, etc.)

6. Applicant's amendment filed October 27, 2006 and other remarks about rejections of the pending claims by using prior art references have been considered but they are not persuasive, and in moot in view of the new ground(s) of rejection.

*** Regarding 35 USC 102 rejection of claims 16-17 by using Egitto (6,826,830):

Applicant alleged (at 10/27/06 remark page 8, last two paragraphs) the meaning of "fill" as to "put into as much as can be held or conveniently contained" and "to supply with a full complement."

In response, claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In Re Self, 213 USPQ 1,5 (CCPA 1982); In Re Priest, 199 USPQ 11,15 (CCPA 1978). Nowhere in independent claims recite pressing the arranged circuit and insulating layers to fully and completely fill the via holes with the conductive paste of the insulating layers.

Applicant then further remarked that the conductive plugs 583 and 584 do not *fill* the via holes of the circuit layers.

In response, this is noted and found unconvincing. It is the fact that, as already shown in Figure 25 of Egitto (6,826,830), at least a portion of the via holes is filled with the conductive paste of the insulating layers. Moreover, as clearly shown in Figure 25 of Egitto, the conductive paste is filled into the via holes by putting the conductive paste into the via holes as much as can be held. Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In Re Self, 213 USPQ 1,5 (CCPA 1982); In Re Priest, 199 USPQ 11,15 (CCPA 1978).

*** Regarding 35 USC 103 rejection of claims 1,9,14,15 by using Egitto (6,826,830) and Furui (5,258,094):

Applicant apparently remarked (at 10/27/06 remark pages 9-10) that there is no suggestion and motivation to combine the references of Egitto (6,826,830) taken with Furui (5,258,094).

In response, this is noted and found totally unconvincing. As already of record, after pressing, desired circuit patterns on the board can be subsequently formed and made for a particular circuit connection. Forming desired circuit patterns on the outermost layer of the board obtained by pressing the circuit layer and the insulating layer is clearly taught by Furui. The examiner recognizes that references cannot be arbitrarily combined and that there must be some logical reason why skilled in the art would be motivated to make the proposed combination of references. In re Regel 188 USPQ 136 (CCPA 1975). The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin 170 USPQ 209 (CCPA 1971): In Re Rosselet 146 USPQ 183 (CCPA 196). References are evaluated by what they collectively suggest to one versed in the art, rather than by their specific disclosures. In Re Simon, 174 USPQ 114 (CCPA 1972); In Re Richman 165 USPQ 509, 514 (CCPA 1970).

Applicant further alleged about the claimed invention that "...placing the necessary conductive layers on the outermost surfaces of the board with which to form any subsequent circuit layers. In the claimed invention, for example, the circuit layers 506a and 506c of FIGURE 8 have a copper plating layer 505 as the outermost layer which is used to form circuit patterns after pressing.

In response, this is noted and found unconvincing. First, nowhere in the claims recites "...placing the necessary conductive layers on the outermost surfaces of the board with which to form any subsequent circuit layers...", and nowhere in the claims recite "a copper plating layer 505 as the outermost layer which is used to form circuit patterns after pressing. Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In Re Self, 213 USPQ 1,5 (CCPA 1982); In Re Priest, 199 USPQ 11,15 (CCPA 1978).

Second, moreover, the rejection is under 35 USC 103 of combined references of Egitto and Furui, in which Furui clearly teaches patterning a necessary conductive layer on the outermost layer of the board in order to form the circuit patterns 61,68 (see Figs 16-17, col 5, lines 49-58, in which the photoresist 7 is used as a mask). This is because of the desirability to form desired circuit patterns on the outermost layer of the board obtained by pressing the circuit layer and the insulating layer, wherein desired circuit patterns on the board can be subsequently formed and made for a particular circuit connection. The rejection is not overcome by pointing out that one reference does not contain a particular limitation when reliance for that teaching is on another reference. In Re Lyons 150 USPQ 741 (CCPA 1966). Moreover, it is well settled that one can not show non-obviousness by attacking the references individually where, as here,

the rejection is based on combinations of references. In Re Keller, 208 USPQ 871 (CCPA 1981); In Re Young, 159 USPQ 725 (CCPA 1968).

** Applicant alleged (at 10/27/06 remark, pages 11-12+) about the rejection using Kim (2004/0194303) Egitto, and Furui that

> ...At paragraph [0039], Kim et al. describes the problem with plugging via holes with paste. So therefore, in order to solve this problem, Kim et al. proposes to omit the paste and instead plat the via holes with copper. This is the explicit object of the invention of Kim et al. described at paragraph [0042]. Therefore, Kim et al. does not teach omitting the paste so that the via holes can be filled during pressing, but instead, Kim et al. teaches omitting the conductive paste and using plated copper in the via hole.

In response, this is noted and found unconvincing. First, it is not disagreed with Applicant that, in a second embodiment of Kim when the diameter of each via holes is relatively small, the via holes are plugged by the electroless-copper plating and electrolytic copper plating (Figs 3C-3D,7), and thus do not need to be subjected to any additional plugging processs, and plugging process of the relatively small via holes may be omitted.

However, the rejection is under 35 USC 103 of Kim, Egitto, and Furui, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Merck & Co., 800 F.2d 1091,231 USPQ 375 (Fed. Cir. 1986). Herein, in the rejection under 35 USC 103, Kim teaches the necessity of filling the via holes with a conductive paste when the diameter of each via holes is large (not relatively small, Figs 2C-2E, paragraphs 60-63, first embodiment). In the same rejection by using the combined references, Egitto then teaches pressing the arranged circuit and insulating layers to fill the via holes of the circuit layers with the conductive paste of the insulating layers during (Figs 24-25). Furui further teaches forming the circuit patterns on the outermost layer of a board obtained by pressing the circuit layers and the insulating layer. Therefore, the subject matter as a whole would have been obvious to one of ordinary skill in the art at the time the invention was made to form multi-layer printed circuit board of Kim by pressing to flow conductive paste from the insulating layer to fill the via holes in the circuit layers during the pressing, as taught by Egitto. This is because of the desirability to provide an electrical connection, wherein the conductive paste are flown into the via holes so that the layers can be effectively joined together. Also, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form multi-layer printed circuit board of Kim by forming circuit patterns on the outermost layers of a board obtained by pressing

the circuit layers and the insulating layers, as taught by Furui. This is because of the desirability to form desired circuit patterns on the outermost layer of the board obtained by pressing the circuit layer and the insulating layer, wherein desired circuit patterns on the board can be subsequently formed and made for a particular circuit connection.

"The use of patents as references is not limited to what the patentees describe as their own inventions or to the problems with which they are concerned. They are part of the literature of the art, relevant for all they contain." In re Heck, 699 F.2d 1331, 1332-33,216 USPQ 1038, 1039 (Fed. Cir. 1983) (quoting In re Lemelson, 397 F.2d 1006, 1009, 158 USPQ 275, 277 (CCPA 1968)). A reference may be relied upon for all that it would have reasonably suggested to one having ordinary skill the art, including nonpreferred embodiments. Merck & Co. v. Biocraft Laboratories, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989). See also Celeritas Technologies Ltd. v. Rockwell International Corp., 150 F.3d 1354, 1361, 47 USPQ2d 1516, 1522-23 (Fed. Cir.1998).

The Examiner recognizes that references cannot be arbitrarily combined and that there must be some logical reason why skilled in the art would be motivated to make the proposed combination of references. In re Regel 188 USPQ 136 (CCPA 1975). The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin 170 USPQ 209 (CCPA 1971): In Re Rosselet 146 USPQ 183 (CCPA 196). References are evaluated by what they collectively suggest to one versed in the art, rather than by their specific disclosures. In Re Simon, 174 USPQ 114 (CCPA 1972); In Re Richman 165 USPQ 509, 514 (CCPA 1970).

Accordingly, the rejections are outstanding and maintained.

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Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The central fax phone number is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).
Oacs-102

Michael Trinh
Primary Examiner